CLAIMS

What is claimed is:

1. A method for forming a diode on a silicon wafer, the method comprising:

forming an active region in the silicon wafer;

forming a first metal silicide layer over said active region;

forming a layer of insulating material over said first refractory metal silicide layer;

etching a diode opening through said layer of insulating material to expose a portion of said first refractory metal silicide layer, wherein said diode opening has an interior surface;

forming a second refractory metal silicide layer over said interior surface of said diode opening;

forming a doped polysilicon plug within said diode opening;

incorporating a platinum silicide layer into said plug, wherein said platinum silicide layer does not contact said second refractory metal silicide layer;

forming an insulative silicon layer on said layer of insulation material and over said diode opening;

opening a passageway through said insulative silicon layer, such that said passageway extends to said platinum silicide layer;

forming a layer of chalcogenide material over said insulative silicon layer and within said passageway, wherein said forming a layer of chalcogenide

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material is performed at least to an extent such that said chalcogenide material contacts said platinum silicide layer;

forming a layer of titanium nitride over said chalcogenide material; and

providing said layer of titanium nitride with a metal contact.

2. A method as recited in Claim 1, wherein said insulative silicon layer comprises silicon nitride.

3. A method as recited in Claim 1, wherein said insulative silicon layer comprises silicon dioxide.

4. A method as recited in Claim 1, wherein said opening a passageway comprises etching through said insulative silicon layer.

5. A method as recited in Claim 1, further comprising doping with a first type dopant the silicon wafer.

6. A method as recited in Claim 1, wherein the silicon wafer has an exposed surface and said forming an active region comprises doping at least a portion of said exposed surface of the silicon wafer with a second type dopant.

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7. A method as recited in claim 1, wherein forming a doped polysilicon plug comprises:

filling said diode opening with doped amorphous silicon; and

converting said doped amorphous silicon to polysilicon.

8. A method as recited in Claim 7, wherein said polysilicon comprises large grain polysilicon.

9. A method as recited in Claim 7, wherein filling said diode opening with doped amorphous silicon comprises:

filling said diode opening with amorphous silicon; and

doping said amorphous silicon with a second type dopant.

10. A method as recited in Claim 1, wherein the silicon wafer has an exposed surface, and further comprising:

doping with a first type dopant the silicon wafer;

doping at least a portion of said exposed surface of the silicon wafer with a second type dopant to form an active region;

filling said diode opening with doped amorphous silicon, wherein said doped amorphous silicon comprises the second type dopant; and

converting said doped amorphous silicon to polysilicon.

11. A method as recited in Claim 10, wherein said polysilicon comprises large grain polysilicon.

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12. A method as recited in Claim 10, wherein said second type dopant provides a conductivity opposite to the conductivity provided by said first type dopant.

13. A method as recited in Claim 10, wherein said first type dopant comprises a P-type dopant.

14. A method as recited in Claim 10, wherein said second type dopant comprises an N-type dopant.

15. A method as recited in Claim 1, wherein said forming a second refractory metal silicide layer comprises:

forming a polysilicon layer on said layer of insulation material and on said interior surface of said diode opening;

forming a refractory metal layer over said polysilicon layer; and

chemically reacting at least a portion of said refractory metal layer with at least a portion of said polysilicon layer to form a second refractory metal silicide layer in said interior surface of said diode opening.

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16. A method for forming a diode on a silicon wafer, the silicon wafer having an exposed surface and being doped with a first type dopant, the method comprising:

highly doping a portion of the exposed surface of the silicon wafer with a second type dopant to form an active region;

disposing a first refractory metal silicide layer over said active region;

forming a layer of insulation material over said first refractory metal silicide layer;

etching a diode opening through said layer of insulation material to expose a portion of said first refractory metal silicide layer, wherein said diode opening has an interior surface;

disposing a second refractory metal silicide layer over said interior surface of said diode opening;

filling said diode opening with amorphous silicon;

lightly doping said amorphous silicon with said second type of dopant;

heating said amorphous silicon to convert said amorphous silicon to large grain polysilicon;

applying a platinum silicide layer to said silicon plug so as to not contact said second refractory metal silicide layer;

positioning an insulative silicon layer on said layer of insulation material and over said diode opening;

etching a passageway through said insulative silicon layer and down to said platinum silicide layer;

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placing a layer of chalcogenide material over said insulative silicon layer and within said passageway so as to contact said platinum silicide layer;

locating a layer of titanium nitride over said chalcogenide material; and

securing a metal contact onto said layer of titanium nitride.

17. A method for forming a diode as recited in Claim 16, wherein said disposing a second refractory metal silicide layer comprises:

covering said layer of insulation material and said interior surface of said diode opening with a polysilicon layer;

applying a refractory metal layer over said polysilicon layer; and

exposing said refractory metal layer to a temperature sufficient to chemically react said polysilicon layer with said refractory metal layer to form a second refractory metal silicide layer positioned over said layer of insulation material and on said interior surface of said diode opening.

18. A method as recited in Claim 16, wherein said second type dopant provides a conductivity opposite to the conductivity provided by said first type dopant.

19. A method as recited in Claim 16, wherein said first type dopant comprises a P-type dopant.

20. A method as recited in Claim 16, wherein said second type dopant comprises an N-type dopant.

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